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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/808,344	03/25/2004	Jun Koyama	0756-7274	5456
31780	7590	06/30/2005	EXAMINER	
ERIC ROBINSON PMB 955 21010 SOUTHBANK ST. POTOMAC FALLS, VA 20165			QUACH, TUAN N	
			ART UNIT	PAPER NUMBER
			2826	

DATE MAILED: 06/30/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	10/808,344	KOYAMA, JUN
	Examiner Tuan Quach	Art Unit 2826

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) Responsive to communication(s) filed on 06 April 2005.
- 2a) This action is FINAL. 2b) This action is non-final.
- 3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) Claim(s) 1-24 is/are pending in the application.
- 4a) Of the above claim(s) 1-6 and 19-24 is/are withdrawn from consideration.
- 5) Claim(s) _____ is/are allowed.
- 6) Claim(s) 7-18 is/are rejected.
- 7) Claim(s) _____ is/are objected to.
- 8) Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) The specification is objected to by the Examiner.
- 10) The drawing(s) filed on 25 March 2004 is/are: a) accepted or b) objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
 - a) All b) Some * c) None of:
 1. Certified copies of the priority documents have been received.
 - Certified copies of the priority documents have been received in Application No. _____.
 - Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)	4) <input type="checkbox"/> Interview Summary (PTO-413)
2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)	Paper No(s)/Mail Date. _____.
3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.	5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152)
	6) <input type="checkbox"/> Other: _____.

DETAILED ACTION

Claims 7-18 are elected without traverse. claims 1-6 and 19-24 are withdrawn from consideration.

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 7-12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Koyama et al. taken with Ogawa et al. and Bird et al.

Re claim 7, Koyama et al. 6,057,183 teaches a driver circuit including a shift register, a buffer circuit connected thereto including a source follower circuit comprising a polysilicon channel thin film transistor, an analog memory electrically connected to the buffer circuit. Koyama lacks primarily the recitation of the thin film transistor is a depletion mode transistor. See Fig. 9, column 1 line 35 to column 2 line 23. Claim 10 recites the same except with the recitation of the product by process limitation of the polysilicon by crystallizing an morphous silicon not deemed patentable given substantially similar structure is disclosed and alternatively, such polysilicon by crystallizing amorphous silicon is notoriously conventional, in any event.

Bird et al. 4,929,884 teaches the use of depletion-mode MOSFETs for applications in very low-power circuits. See column 9 line 64 to column 9 line 4.

Ogawa et al. 6,127,857 teaches the use of depletion-mode FETS to reduce power and enhance accuracy in the buffer circuit. See column 4 line 33 to column 5 line

35, column 6 lines 16-64. The provision of the polysilicon thin film transistor is also apparent, e.g., Fig. 13,

It would have been obvious to one skilled in the art in practicing the above invention to have employed the thin-film transistors of depletion mode to obtain low power and or enhance accuracy in the buffer circuit as evidenced by Bird et al. or Ogawa et al.

Regarding claims 8 and 11, the connection of the thin film transistor to an output terminal for electrical connection is well within the purview of one skilled in the art and as evidenced by Ogawa et al., column 6 line 21. Regarding claims 9 and 12, the provision or selection of suitable substrates such as quartz or glass substrate is well within the purview of one skilled in the art, e.g., Koyama et al., column 1 lines 55-59, Ogawa et al., column 16 lines 1-2 and as such would have been obvious.

Claims 13-18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Koyama et al. taken with Ogawa and Bird et al. and further in view of Fujikura.

Re claim 13 and 16, Koyama et al. is applied as above and additionally does not recite the buffer circuit comprising a bootstrap circuit comprising the thin film transition in a depletion mode transistor. The product-by-process recitation of the polysilicon by crystallizing amorphous silicon is treated as with regard to claim 10 above.

Ogawa et al. and Bird et al. are applied as above.

Fujikura 5,949,271 teaches the shift register circuit or buffer circuit including a bootstrap circuit including thin film transistors. See column 1 lines 6 to column 2 line 18,

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column 8 lines 6-48, column 13 lines 26-43. The advantages include buffer or shift register circuit capable of operating at high speed.

Accordingly, it would have been obvious to have incorporated the bootstrap circuit in the above structure wherein such would have been advantageous to obtain buffer circuit capable of operating at high speed. The use of depletion-mode would have been conventional and obvious as evidenced by Ogawa et al. and Bird et al. as delineated above to obtain low power and/or enhance accuracy in the buffer circuit,

The connection to output terminal in claims 14 and 17, and the employment of suitable substrates such as glass or quartz in claims 15 and 18 would have been obvious for the same reasons delineated with regard to claims 8 and 11, and 9 and 12, respectively, above.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to examiner Tuan Quach whose telephone number is 571-272-1717. The examiner can normally be reached on M-F from 8:30 AM to 4:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor Nathan Flynn, can be reached on 571-272-1915. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should

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you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



Tuan Quach
Primary Examiner